Serial No.: 10/051,062
Docket No.: NEG-241
KATO.021

REMARKS

Claims 1-30 are presently pending in the application. Independent claims 1, 4, 7, 10, 15, 19, 23, and 27 have been amended to more particularly define the invention.

Claims 1, 4, 7, 10, 13-15, 19, 23 and 27 were rejected under 35 U.S.C. §103(a) as being unpatentable over Chen, U.S. Patent No. 5,544,332, in view of Gibson, U.S. Patent No. 6,553,512. Objection was made to claims 2-3, 5-6, 8-9, 11-12, 16-18, 20-22, 24-26 and 28-30, with the indication that these claims would be allowable if rewritten in independent form. However, Applicant submits that all the claims are allowable. Consequently, the rejection is respectfully traversed.

In the claimed invention, a command from a processor unit is to be executed on a PCI bus which has a plurality of PCI devices connected to it. A PCI bus monitoring circuit monitors target operating signals from PCI devices which operate as PCI target devices. These target devices thus can execute the command. In some exemplary embodiments of the invention, if plural PCI target devices respond to the command in one cycle, the PCI bus monitoring circuit sends an error report signal to the processor unit. In other exemplary embodiments of the invention, the PCI bus monitoring circuit includes a unit for resetting the PCI bus when plural PCI target devices respond to the command in one PCI cycle.

In all embodiments of the claimed invention, the command is from the processor unit, and it is responses to the command from plural PCI target devices that result in an error report signal or in resetting the PCI bus.

Chen discloses a multi-bus system which detects a potential arbitration deadlock condition between two masters, coupled to different buses, seeking control of one slave

connected to one of the buses. Chen's system includes plural masters on two buses, plural slaves on the same bus as one of the masters, and a masking and deadlock detection system which is responsive to a master on a first one of the buses seeking access to a slave on a second bus at a time when a master on the second bus has access to that slave. If such a deadlock is detected, a "relinquish and retry" signal is generated, blocking the master on the second bus from seeking another access to the slave for a random period of time. See Chen at column 3, line 65 to column 4, line 28.

Chen also discloses that the prior art includes a system having plural masters on two buses, plural slaves on the same bus as one of the masters, and a bus coupler that includes a bus arbiter, and a bus protocol for each bus.

The final rejection contends that Chen discloses a system comprising plural PCI devices, which the final rejection identifies as masters. The final rejection then contends that each of these masters, when operating as a PCI master device, activates a corresponding master operating signal. Assuming this to be Chen's disclosure, even so, it teaches away from the claimed invention in which plural PCI devices, when acting as PCI target devices, activate corresponding target operating signals.

The final rejection continues by contending that in Chen's system, a deadlock is detected when plural master devices respond in one PCI cycle. However, at column 3, line 65 to column 4, line 12, Chen states that a potential arbitration deadlock condition arises when two masters coupled to different buses seek control of one slave connected to one of the buses. Thus, the masters are not responding, they are initiating action – seeking control of the one slave.

Chen goes on to state that a potential arbitration deadlock for control of a bus occurs when a first master coupled to a first bus attempts to access a slave on a second bus, but is prevented from doing so because the arbiter for the second bus continues to grant control of the second bus to a second master connected to the second bus. Thus, the first master is initiating action by seeking access.

At column 4, lines 21-27, Chen states that once his deadlock detection and masking block detects a potential arbitration deadlock, a masking system prohibits the second master from gaining control of the second bus. Thus, Chen does not monitor target operating signals. If anything, Chen responds to source signals to detect a potential deadlock.

In short, Chen's masters are not targets for commands; they are sources of signals, which may be commands. Chen's masking and deadlock detection system does not monitor target addresses or target operating signals; instead, it monitors masters which seek access to a slave.

The independent claims, and thus all the claims, include that the PCI bus monitor circuit monitors a target address of a command from the processor unit, and that the PCI bus monitor circuit takes action when plural PCI target devices respond to the command in one PCI cycle.

As set forth above, during the interview, Examiner Baderman agreed that amended claim 1 appears to overcome the rejection based on Chen. The other independent claims have been amended in the same way, thus also avoiding Chen.

Gibson discloses a method and an apparatus for resolving CPU deadlocks. Gibson states that a deadlock may occur when code makes reference to a non-existent memory, and

that one way to resolve deadlocks is to issue an error signal and restart the CPU. Gibson does not provide that which distinguishes the claims from Chen, as discussed above.

In view of the foregoing, Applicant submits that claims 1-30, all the claims presently pending in the application, are patentably distinct over the prior art of record and are allowable, and that the application is in condition for allowance. Such action would be appreciated.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned attorney at the local telephone number listed below to discuss any other changes deemed necessary for allowance in a telephonic or personal interview.

To the extent necessary, Applicant petitions for an extension of time under 37 CFR §1.136. The Commissioner is authorized to charge any deficiency in fees, including extension of time fees, or to credit any overpayment in fees to Attorney's Deposit Account No. 50-0481.

Respectfully Submitted,

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CERTIFICATE OF FACSIMILE TRANSMISSION

I hereby certify that I am filing this Amendment Under 37 C.F.R. §1.116 by facsimile with the United States Patent and Trademark Office to Examiner Scott T. Baderman, Group Art Unit 2113, at fax number (703) 872-9306 this 22th day of June 2005.

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